



## SDR DESIGN BENCH (SDB05) SPECIFICATION

### Hardware

- SDR Transmitter
- SDR Receiver
- USB to JTAG programming cable - 2 Nos
- Patch Antenna - 2 Nos, Cables.

### Software

- VHDL files for ASK, FSK, QPSK, BPSK & QAM modulation.
- VHDL files for FSK demodulation.
- Bit files for QPSK demodulation.
- Software control interface for RF frequency and power selection.(VHDL Files).
- PC Interface for RS232 data communication. (OS-Windows only).

### Add On Modules

- Audio codec.\*
- Video codec.\*

### Features

- FPGA based board with 1.5 million gates (Spartan 3XC3S1500)
- High speed Analog I/O Module (ADC & DAC)
- RF Transceiver with 2.4 Ghz to 2.5 GHz RF output
- Variable RF channel and power selection
- Zero IF down conversion
- Built in Multi output Power supply for FPGA, RF and Analog I/O Module.
- USB to JTAG cable for downloading the VHDL codes to the Spartan-3 board.

## Technical Specifications for SDR Transmitter and Receiver

### Spartan 3 (Device: XC3S1500 - 4FG676)

- Upto 208K Distributed RAM
- Upto 576K Embedded block RAM
- 32 18x18 Multipliers
- 487 Single ended 221 differential pair I/Os.
- Clock:1.5MHz to 170MHz
- Built in RS232, USB ports.
- Upto 4 DCM'S

### Analog Module

- Two 12Bit 53 MSPS A/D converters
- AC coupled single ended 1 to 1.5 Vpp analog input.
- Input Low Pass Filter with  $f_c=19.4\text{MHz}$ .
- Two 12 bit 165MSPS D/A converters
- Single ended, 2 Volt analog output.
- Output Low Pass Filter with  $f_c = 28.4\text{MHz}$

### RF Transceiver

- 2.4GHz to 2.5GHz ISM Band operation.
- 802.11b PHY compatible.
- Integrated +17 dBm Power Amplifier.
- Integrated Transmit/Receive Switch.
- Complete RF to Baseband Transceiver
  - Direct up/down conversion
  - Monolithic low phase noise VCO
  - Integrated Baseband LPF
  - Integrated PLL with 3 wire serial interface
  - Digital bias control for power Amplifier
  - Transmit power control
  - Complete Baseband interface
- 95 dbm receiver sensitivity at 1 MBPS
- Single +2.7V to +3.6V power supply



### Note:

The institution should provide Original Xilinx ISE foundation and Chipscope pro for compiling all VHDL library files and viewing all FPGA signals like ADC input.

\* Ask for Separate Quotation. Audio and video Codec with accessories are also available as Add-on for SDR

### Contact